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BROOKS, SHANNON	
ART UNIT	**PAPER NUMBER**
2617	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/753,005	Applicant(s) KIM ET AL.	
	Examiner Shannon R. Brooks	Art Unit 2617	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 1-31** rejected under 35 U.S.C. 103(a) as being unpatentable over Sinha (US 2004/0152418 A1) in view of Webster (US 2003/0072284 A1).

Consider **Claim 1**, Sinha teaches a physical layer unit for a wireless Local Area Network (LAN) system, the physical layer unit comprising: an Analog-to-Digital (A/D) converter that receives and converts an OFDM analog signal or a DSSS/CCK analog signal processed by an RF module into a digital signal **(Pg. 3, [0031]-[0033])**; and a receiving processor that: interpolates **(read as changes the sampling rate, Pg. 5, [0047])** and demodulates the converted digital signal **(Pg. 5, [0051])**, filters the interpolated and demodulated signal as a DSSS/CCK demodulation

signal **(Pg. 5, [0052])**; and directly demodulates the converted digital signal without interpolation **(read as in a zero-IF receiver, Pg. 4, [0035])**, and filters the demodulated signal as an OFDM demodulation signal **(Pg. 3, [0032])** .

Sinha teaches filtering the demodulated signals and does not specifically in detail teach outputting the signals. However, Webster teaches outputting the signals (Pg. 5, [0045]. Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Webster into Sinha in order to aid in the mixing process (Pg. 5, [0045])

Consider **Claim 5**, Sinha teaches a physical layer unit for a wireless LAN system, the physical layer unit comprising: an Analog-to-Digital (A/D) converter that receives and converts an OFDM analog signal or a DSSS/CCK analog signal processed by an RF module into a digital signal **(Pg. 3, [0031]-[0033])**; and a receiving processor that demodulates the converted digital signal as an OFDM demodulation signal and filters the OFDM demodulation signal according to a predetermined DSSS/CCK control in response to signal determination flag **(read as provide a control signal)** information in a first logic state, **(Pg. 5, [0051])**; and that demodulates and filters the converted digital signal as a DSSS/CCK demodulation signal according to a predetermined DSSS/CCK control in response to signal determination flag information **(read as provide a control signal)** in a second logic state **(Pg. 5, [0052])**.

Sinha teaches filtering the demodulated signals and does not specifically in detail teach outputting the signals. However, Webster teaches outputting the signals (Pg. 5, [0045]. Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Webster into Sinha in order to aid in the mixing process (Pg. 5,

[0045])

Consider **Claim 12**, Sinha teaches a wireless LAN system comprising: an RF module that receives an OFDM modulation signal or a DSSS/CCK modulation signal as an analog signal and filters an OFDM analog signal or a DSSS/CCK analog signal **(read as zero-IF receiver, Pg. 4, [0035])**; a physical layer unit that receives and converts an analog signal filtered from the RF module into a digital signal, interpolates and demodulates the digital signal, filters the interpolated and demodulated signal as a DSSS/CCK demodulation signal, and directly demodulates **(read as zero-IF, Pg. 4, [0035])** and filters the digital signal as an OFDM demodulation signal **(Pg. 5, [0050]-[0054] and Pg. 6, [0056]-[0057])**.

Sinha teaches filtering the demodulated signals and does not specifically in detail teach outputting the signals. However, Webster teaches outputting the signals (Pg. 5, [0045]. Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Webster into Sinha in order to aid in the mixing process (Pg. 5, [0045])

Consider **Claim 17**, Sinha teaches a wireless LAN system comprising: an RF module that receives an OFDM modulation signal or a DSSS/CCK modulation signal as an analog signal and filters an OFDM analog signal or a DSSS/CCK analog signal **(read as zero-IF receiver, Pg. 4, [0034])**; a physical layer unit that receives and converts an analog signal filtered from the RF module into a digital signal, filters the converted digital signal as an OFDM demodulation signal, according to a predetermined DSSS/CCK control, in response to signal determination flag information **(read as control signal)** in a first logic state, the signal determination flag information being set by processing the converted digital signal, and demodulates and filters the

converted digital signal as a DSSS/CCK demodulation signal, according to the predetermined DSSS/CCK control, in response to signal determination flag information **(read as control signal)** in a second logic state**(Pg. 5, [0050]-[0054] and Pg. 6, [0056]-[0057])** ; and a MAC layer unit that link-distributes the DSSS/CCK demodulation signal or the OFDM demodulation signal to other interfaced external layers **(read as layers with controllable switches, Pg. 2, [0015] or antennas, Fig. 2).**

Sinha teaches filtering the demodulated signals and does not specifically in detail teach outputting the signals. However, Webster teaches outputting the signals (Pg. 5, [0045]. Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Webster into Sinha in order to aid in the mixing process (Pg. 5, [0045]).

Consider **Claim 25**, Sinha teaches an wireless LAN method, which is implemented on a wireless LAN system, comprising: receiving a radio wave and extracting and filtering an OFDM analog signal or a DSSS/CCK analog signal **(Pg. 2, [0009]-[0011])**; converting the analog signal into a digital signal **(Pg. 2, [0009]-[0011])**; interpolating the converted digital signal **(read as changes the sampling rate, Pg. 5, [0047])**; demodulating the interpolated signal as a DSSS/CCK demodulation signal **(Pg. 5, [0052])**; directly demodulating (read as zero-IF conversion, Pg. 4, [0035]) and filteringting the converted digital signal as an OFDM demodulation signal (Pg. 5, [0051]-[0055] and Pg. 6, [0056]-[0057]); and link-distributing one of the DSSS/CCK demodulation signal and the OFDM demodulation signal to other interfaced external layers **(read as layers with controllable switches, Pg. 2, [0015] or antennas, Fig. 2)**.

Sinha teaches filtering the demodulated signals and does not specifically in detail teach outputting the signals. However, Webster teaches outputting the signals (Pg. 5, [0045]. Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Webster into Sinha in order to aid in the mixing process (Pg. 5, [0045])

Consider **Claim 27**, Sinha teaches a wireless LAN method, which is implemented on a wireless LAN system, comprising: receiving a radio wave, and extracting and filtering an OFDM analog signal and a DSSS/CCK analog signal **(Pg. 5, [0051]-[0055] and pg. 6, [0056]-[0057])**; converting the analog signal into a digital signal **(Pg. 5, [0051]-[0055] and pg. 6, [0056]-[0057])**; processing the converted digital signal **(Pg. 5, [0051]-[0055] and pg. 6, [0056]-[0057])** and setting the state of signal determination flag information **(read as control signal, Pg. 5, [0051] and [0052])** ; filtering the converted digital signal as an OFDM demodulation signal **(Pg. 5, [0051])** in response to signal determination flag information in a first logic state **(read as control signal, Pg. 5, [0051])**; performing a predetermined DSSS/CCK control **(Pg. 5, [0052])** corresponding to the signal determination flag information **(read as control signal, Pg. 5, [0052])**; demodulating and filtering the converted digital signal as an DSSS/CCK demodulation signal, according to the predetermined DSSS/CCK control, in response to signal determination flag information in a second logic state **(Pg. 5, [0052])**; and link-distributing the DSSS/CCK demodulation signal or the OFDM demodulation signal to other interfaced external layers **(read as layers with controllable switches, Pg. 2, [0015] or antennas, Fig. 2.)**

Sinha teaches filtering the demodulated signals and does not specifically in detail teach outputting the signals. However, Webster teaches outputting the signals (Pg. 5, [0045].

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Webster into Sinha in order to aid in the mixing process (Pg. 5, [0045])

Consider **Claim 2**, Sinha teaches the physical layer unit of claim 1, further comprising; a Physical Layer Convergence Protocol (PLCP) processor which receives a DSSS/CCK demodulation signal, an OFDM demodulation signal, and classifies the received signals according to an OFDM standard or a DSSS/CCK standard **(Pg. 5, [0050]-[0055] and Pg. 6, [0056]-[0057])**, relays the classified signals to respective corresponding upper layers using a PLCP **(read as identifies received packets for needed circuitry, Pg. 3, [0025])**, and performs general control operations **(read as through control signals, Pg. 5, [0051] and [0052])**; and a transmitting processor which receives a packet signal output from the PLCP processor, performs OFDM modulation or DSSS/CCK modulation of the packet signal **(Pg. 6, [0059])**, and filters the modulated signal as an OFDM analog signal or a DSSS/CCK analog signal to the RF module **(Pg. 6, [0060])**, wherein the transmitting processor comprises: a DSSS/CCK modulator which receives and modulates a packet signal of a DSSS/CCK standard, and filters the modulated signal as a DSSS/CCK modulation signal **(Pg. 6, [0059] and [0060])**; an OFDM modulator which receives and modulates a packet signal of an OFDM standard, and filters the modulated signal as an OFDM modulation signal **(Pg. 6, [0059] and [0060])**; a multiplexing (MUX) unit which filters one of the DSSS/CCK modulation signal and the OFDM modulation signal according to a processing sequence (Pg. 7, [0072]); and A D/A converter which converts a signal filtered from the MUX unit into an analog signal and filters the converted signal as the OFDM analog signal or the DSSS/CCK analog signal **(Pg. 7, [0072] and Pg. 8, [0073]-[0077])**.

Consider **Claim 3**, Sinha teaches the physical layer unit of claim 1, wherein the receiving processor comprises: the A/D converter that receives and converts the analog signal processed by the RF module into the digital signal **(Pg. 3, [0029]-[0031])**; an interpolation unit that interpolates and filters the converted digital signal **(read as up samples, Pg. 5, [0046]-[0049])**; a DSSS/CCK demodulator which demodulates the interpolated signal and filters the demodulated signal as the DSSS/CCK demodulation signal **(Pg. 5, [0052])**; and an OFDM demodulator which directly demodulates the converted digital signal and filters the demodulated signal as the OFDM demodulation signal **(Pg. 5, [0051])**.

Consider **Claim 4**, Sinha teaches, the physical layer unit of claim 1, wherein the interpolation is performed by synchronizing the converted digital signal to a sampling clock corresponding to a transmission rate of the DSSS/CCK standard and approximating the synchronized digital signal using a third-order or a higher order function **(read as fourth-order function, Table 1, Pg. 8)**.

Consider **Claim 6**, Sinha teaches the physical layer unit of claim 5, further comprising: a Physical Layer Convergence Protocol (PLCP) processor which receives a DSSS/CCK demodulation signal, a OFDM demodulation signal, and classifies the received signals according to an OFDM standard or a DSSS/CCK standard, relays the classified signals to respective corresponding upper layers using a PLCP, and performs general control operations **(Pg. 5, [0050]-[0055] and Pg; 6, [0056] and [0057])** and a transmitting processor which receives a packet signal output from the PLCP processor, performs OFDM modulation or DSSS/CCK

modulation of the packet signal **(Pg. 6, [0059])**, and filters the modulated signal as an OFDM analog signal or a DSSS/CCK analog signal **(Pg. 6, [0059] and [0060])**; wherein the transmitting processor comprises: a DSSS/CCK modulator which receives and modulates a packet signal of a DSSS/CCK standard, and filters the modulated signal as a DSSS/CCK modulation signal **(Pg. 6, [0059] and [0060])**; an OFDM modulator which receives and modulates a packet signal of an OFDM standard, and filters the modulated signal as an OFDM modulation signal **(Pg. 6, [0059] and [0060])**; a MUX unit which outputs one of the DSSS/CCK modulation signal and the OFDM modulation signal according to a processing sequence **(Pg. 7, [0072])**; and a D/A converter which converts a signal filtered from the MUX unit into an analog signal, and filtereds the converted analog signal as the OFDM analog signal or the DSSS/CCK analog signal **(Pg. 7, [0072] and Pg. 8, [0073]-[0077])**.

Consider **Claim** 7, Sinha teaches the physical layer unit of claim 5, wherein the receiving processor comprises: the A/D converter that receives the analog signal processed by the RF module and converts the received analog signal into the digital signal **(Pg. 3, [0031]-[0033])**; a DSSS/CCK controller which performs the predetermined DSSS/CCK control corresponding to the signal determination flag information **(read as control signal)** and controls an output of the converted digital signal **(Pg. 5, [0052])**; an OFDM demodulator which demodulates the converted digital signal, sets the signal determination flag information (read as control signal) to a first logic state **(Packet indicator)** or a second logic state **(disabler)**, and filters the demodulated signal as the OFDM demodulation signal in response to the signal determination flag information set to the first logic state **(Pg. 5, [0051])**; and a DSSS/CCK demodulator which filters the demodulated signal as the DSSS/CCK demodulation signal in response to the signal

determination flag information set to the second logic state **(Pg. 5, [0052])**.

Consider **Claim 8**, Sinha teaches the physical layer unit of claim 5, wherein the predetermined DSSS/CCK control is performed to allow the DSSS/CCK demodulator to conduct a preamble processing of the received signal within a predetermined second time period after the signal determination flag information is set to the second logic state within a predetermined first time period for preamble processing and detection of a converted digital signal corresponding to the OFDM standard **(Pg. 5, [0050]-[0055] and Pg. 6, [0056]-[0057])**.

Consider Claim 9, Sinah teaches the physical layer unit of claim 5, wherein the signal determination flag information is maintained in the first logic state if the converted digital signal subjected to the preamble processing corresponds to an OFDM standard, and is set to the second logic state if the converted digital signal subjected to the preamble processing does not correspond to the OFDM standard **(Pg. 5, [0050]-[0055] and Pg. 6, [0056]-[0057])**.

Consider **Claim 10**, Sinha teaches the physical layer unit, wherein except thai it does not specifically teach the physical layer wherein the predetermined second time period is 40 .mu.s.

However, Webster teaches the physical layer wherein the predetermined second time period is 40 .mu.s **(Pg. 4, [0041]-[0042] and Pg. 5, [0043] and Fig. 1).**
Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Webster into Sinhar to facilitate synchronization (Pg. 5, [0043].

Consider **Claim 11**, Sinha teaches the physical layer unit , wherein except that it does not specifically teach the physical layer wherein the predetermined first time period is 16 .mu.s.

However, Webster teaches the physical layer wherein the predetermined first time period is 16.mu.s **(Pg. 4, [0041]-[0042] and Pg. 5, [0043] and Fig. 1).**

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Webster into Sinhar to facilitate synchronization (Pg. 5, [0043].

Consider **Claim 13**, Sinha teaches the wireless LAN system of claim 12, further comprising a MAC layer which receives and processes information from other interfaced external layers according to a MAC protocol, outputs the packet signal, receives and link-distributes the DSSS/CCK demodulation signal or the OFDM demodulation signal, and outputs the link-distributed signal to the other interfaced external layers **(read as transmits and receives packets, Fig. 2 and Fig 3)**; and wherein the physical layer unit comprises: a Physical Layer Convergence Protocol (PLCP) processor that receives the packet signal and the demodulation signal, respectively, classifies the received signals according to an OFDM standard or a DSSS/CCK standard **(Pg. 5, [0050]-[0055] and Pg. 6, [0056]-[0057])**, relays the classified signals to respective corresponding upper layers using a PLCP **(read as identifies received packets for needed circuitry, Pg. 3, [0025])**, and performs general control operations **(read as through control signals, Pg. 5, [0051] and [0052])**; a transmitting processor which receives the packet signal output from the PLCP processor, performs OFDM modulation or DSSS/CCK modulation of the packet signal **(Pg. 6, [0059])**, and filters the modulated signal as an OFDM analog signal or a DSSS/CCK analog signal **(Pg. 6, [0060])**, and a receiving processor which receives and converts the analog signal filtered from the RF module into the digital signal, interpolates and demodulates the converted digital signal, filters the interpolated and demodulated signal as the DSSS/CCK demodulation signal to the PLCP processor **(Pg. 5, [0050]-[0055] and Pg. 6, [0056] and [0057])**, and directly demodulates and filters the converted digital signal as the OFDM demodulation signal to the PLCP processor **(read as direct**

conversion, Pg. 4, [0035]).

Consider **Claim 14**, Sinha teaches the LAN system of claim 13, wherein the transmitting processor comprises: a DSSS/CCK modulator which receives and modulates the packet signal of the DSSS/CCK standard and filters the modulated signal as the DSSS/CCK modulation signal **(Pg. 6, [0059])**; an OFDM modulator which receives and modulates the packet signal of the OFDM standard and filters the modulated signal as the OFDM modulation signal **(Pg. 6, [0059])**; a MUX unit that filters one of the DSSS/CCK modulation signal or the OFDM modulation signal according to a processing sequence **(Pg. 7, [0072])**; and a D/A converter that converts a signal filtered from the MUX unit into an analog signal and filters the converted analog signal as the OFDM analog signal or the DSSS/CCK analog signal **(Pg. 7, [0071]-[0072] and Pg. 8, [0073]-[0077])**.

Consider **Claim 15**, Sinha teaches the wireless LAN system of claim 12, wherein the physical layer unit comprises: an Analog-to-Digital (A/D) converter that receives and converts an analog signal filtered from the RF module into a digital signal **(Pg. 4, [0037]-[0041])**; an interpolation unit that interpolates the digital signal **(read as up sampler, Pg. 5, [0046]-[0049])**; a DSS/CCK demodulator which demodulates the interpolated signal and filters the demodulated signal as the DSSS/CCK demodulation signal **(Pg. 5, [0052]);** and an OFDM demodulator which directly demodulates **(read as zero-IF receiver, Pg. 4, [0035])** the converted digital signal and filters the demodulated signal as the OFDM demodulation signal **(Pg. 5, [0051])**.

Consider **Claim 16**, Sinha teaches the wireless LAN system of claim 12, wherein the interpolation **(read as up sampler, Pg. 5, [0047])** is performed by synchronizing the converted digital signal to a sampling clock corresponding to a transmission rate of the DSSS/CCK

standard and approximating the synchronized digital signal using a third-order or a higher-order function **(read as fourth-order function, Table 1, Pg. 8)**.

Consider **Claim18**, Sinha teaches The wireless LAN system, wherein the physical layer unit comprises: a receiving processor that receives an analog signal output from the RF module, converts the analog signal into a digital signal, and demodulates and filters the digital signal as a DSSS/CCK demodulation signal, according to a predetermined DSSS/CCK control corresponding to signal determination flag information **(read as control signal)** and demodulates and filters the converted digital signal as an OFDM demodulation signal in response to signal determination flag information with a first logic state created by processing the converted digital signal **(Pg. 5, [0050]-[0055] and Pg. 6, [0056]-[0057]).**

Consider **Claim 19**, Sinha teaches the wireless LAN system of claim 17 wherein the physical layer unit comprises: a Physical Layer Convergence Protocol (PLCP) processor which receives the demodulation signal, classifies the received signal according to an OFDM standard or a DSSS/CCK standard **(Pg. 5, [0050]-[0055] and Pg. 6, [0056]-[0057])**, relays the classified signal to respective corresponding upper layers using a PLCP PLCP **(read as identifies received packets for needed circuitry, Pg. 3, [0025])**, and performs general control operations**(read as through control signals, Pg. 5, [0051] and [0052])**; and a transmitting processor which receives a packet signal output from the PLCP processor, performs OFDM demodulation or DSSS/CCK modulation of the packet signal **(Pg. 6, [0059])**, and filters the modulated signal as an OFDM analog signal or a DSSS/CCK analog signal **(Pg. 6, [0060])**; and wherein the transmitting processor includes: a DSSS/CCK modulator which receives and modulates the packet signal of the DSSS/CCK standard and filters the modulated signal as a DSSS/CCK modulation signal **(Pg.**

6, [0059] and [0060]); an OFDM modulator which receives and modulates the packet signal of the OFDM standard and filters the modulated signal as an OFDM modulation signal **(Pg. 6, [0059] and [0060])**; a MUX unit that filters one of the DSSS/CCK modulation signal or the OFDM demodulation signal according to a processing sequence **(Pg. 7, [0072]);** and a D/A converter that converts a signal filtered from the MUX unit into an analog signal and filters the analog signal as an OFDM analog signal or an DSSS/CCK analog signal l **(Pg. 7, [0072] and Pg. 8, [0073]-[0077])**..

Consider **Claim 20**, Sinha teaches the wireless LAN system of claim 18, wherein the receiving processor comprises: an A/D converter that receives an analog signal filtered from the RF module and converts it into a digital signal **(Pg. 4, [0037]-[0040])**; an OFDM demodulator which demodulates the converted digital signal, sets the signal determination flag information, and filters the demodulated signal as the OFDM demodulation signal in response to the signal determination flag information in the first logic state **(Pg. 5, [0051]);** a DSSS/CCK controller that performs the predetermined DSSS/CCK control corresponding to the state of the signal determination flag information **(Pg. 5, [0052]);** a DSSS/CCK demodulator which demodulates and filters a signal filtered from the DSSS/CCK controller as a DSSS/CCK demodulation signal **(Pg. 5, [0052])**.

Consider **Claim 21**, Sinha teaches the wireless LAN system of claim 17, wherein the signal determination flag information (read as control signal) is maintained in a first logic state if the converted digital signal subjected to the preamble processing corresponds to an OFDM standard, and is set to a second logic state within a predetermined first time period if the converted digital signal subjected to the preamble processing does not correspond to the OFDM

standard **(Pg. 5, [0050]-[0055] and Pg. 6, [0056]-[0057])**.

Consider **Claim 22**, Sinha teaches the wireless LAN system of claim 21, wherein the predetermined DSSS/CCK control is performed to allow the DSSS/CCK demodulator to perform a second preamble processing of the received signal within a predetermined second time period after the signal determination flag information is set to the second logic state **(Pg. 5, [0050]-[0055] and Pg. 6, [0056]-[0057])**.

Consider **Claim 23**, Sinha teaches the wireless LAN system , except that it does not specifically teach the wireless LAN system wherein the predetermined second time period is 40 .mu.s.

However, Webster teaches the wireless LAN system wherein the predetermined second time period is 40 .mu.s **(Pg. 4, [0041]-[0042] and Pg. 5, [0043] and Fig. 1).** Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Webster into Sinhar to facilitate synchronization (Pg. 5, [0043].

Consider **Claim 24**, Sinha teaches the wireless LAN system , except that it does not specifically teach the wireless LAN system wherein the predetermined first time period is 16 .mu.s.

However, Webster teaches the wherein the wireless LAN system predetermined second time period is 16 .mu.s **(Pg. 4, [0041]-[0042] and Pg. 5, [0043] and Fig. 1).** Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Webster into Sinha to facilitate synchronization (Pg. 5, [0043].

Consider **Claim 26**, Sinha teaches the wireless LAN method of claim 25, wherein the interpolation **(read as up sampler, Pg. 5, [0047])** is performed by synchronizing the converted

digital signal to a sampling clock corresponding to a transmission rate of the DSSS/CCK standard and approximating the synchronized digital signal using a third-order or a higher-order function **(read as fourth-order function, Table 1, Pg. 8)**.

Consider **Claim 28**, Sinha teaches the wireless LAN method of claim 27, wherein the signal determination flag information **(read as control signal)** is maintained in the first logic state if the converted digital signal subjected to a first preamble processing corresponds to an OFDM standard, and the signal determination flag information is set to the second logic state, if the converted digital signal subjected to the first preamble processing does not correspond to the OFDM standard **(Pg. 5, [0050]-[0055] and Pg. 6, [0056]-[0057])**.

Consider **Claim 29**, Sinha teaches the wireless LAN method of claim 28, wherein the predetermined control is performed to allow the DSSS/CCK demodulator to perform a preamble processing of the received signal within a predetermined second time period after the signal determination flag information is set to the second logic state **(Pg. 5, [0050]-[0055] and Pg. 6, [0056]-[0057])**.

Consider **Claim 30**, Sinha teaches the wireless LAN method, except that it does not specifically teach the wireless LAN method wherein the predetermined second time period is 40 .mu.s.

However, Webster teaches the wireless LAN method wherein the predetermined second time period is 40 .mu.s **(Pg. 4, [0041]-[0042] and Pg. 5, [0043] and Fig. 1)**.

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Webster into Sinha to facilitate synchronization (Pg. 5, [0043].

Consider **Claim 31**, Sinha teaches the wireless LAN method, except that it does not

specifically teach the wireless LAN method wherein the predetermined first time period is 16 .mu.s.

However, Webster teaches the wireless LAN method wherein the predetermined second time period is 16 .mu.s **(Pg. 4, [0041]-[0042] and Pg. 5, [0043] and Fig. 1).**

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Webster into Sinha to facilitate synchronization (Pg. 5, [0043].

Conclusion

Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

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Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shannon Brooks whose telephone number is (571) 270-1115. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nick Corsaro can be reached on (571) 272-7876. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Shannon R. Brooks

February 5, 2007

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